Traffic Measurement for AN2/SONET Gateway

Christopher Iyawe
Srii Seetharam
Joseph B. Evans

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Telecommunications and Information Sciences Laboratory
The University of Kansas Center for Research, Inc.
2291 Irving Hill Road
Lawrence, Kansas 66045
TRAFFIC MEASUREMENT FOR AN2/SONET GATEWAY

BY

CHRISTOPHER IYawe
TENNESSEE STATE UNIVERSITY, NASHVILLE

RESEARCH EXPERIENCES FOR UNDERGRADUATES (R.E.U)
ELECTRICAL AND COMPUTER ENGINEERING
THE UNIVERSITY OF KANSAS

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SPONSOR: PROF. EVANS.
GRADUATE STUDENT: SRINI SEETHARAM.

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Introduction:

With computer communication networks reaching transmission capacities exceeding a gigabit per second, it becomes necessary to determine the load on the network. One can measure the flow of traffic and compute statistics from these measurements. The objective of the AN2/SONET project is to design a gateway that will link an experimental Local Area Network (LAN) from Digital Equipment Corporation's System Research center and a gigabit Wide Area Network (WAN) from Sprint, based on evolving Broadband Integrated Service Digital Network (Broadband ISDN).

The research work focuses on advancing the gateway technology that is used to connect Asynchronous Transfer Mode (ATM) high speed Local Area Networks and Synchronous Optical Network (SONET) long distance wide area networks as part of the Multi-Applications and Gigabit Internetwork Consortium (MAGIC). The MAGIC network will connect the University of Kansas in Lawrence, Sprint in Kansas City, the battle command and control battle Laboratory in Fort Leavenworth, Kansas, the Earth Resources Observation System Data Center in Sioux Falls, South Dakota, and the Minnesota Supercomputer center in Minneapolis. The MAGIC network will span approximately 1000km and operate at 2.4Gb/s. This gigabit network will facilitate computational research, remote access to large databases, and visualization in scientific computing.
The ATM Cell:

My work was on the ATM side of the Gateway. ATM is a protocol in which the information is organised into cells. It is asynchronous in the sense that the recurrence of the cells containing information from an individual user is not necessarily periodic. ATM is connection oriented. All cell belong to a pre-established virtual connection. All traffic is segmented into cells for transmission across the ATM network. The ATM standard for broadband ISDN defines a cell of length 53 bytes comprising 5 bytes of header and a payload of 48 bytes as shown on the next page. Each cell header contains a virtual channel identifier (VCI) to identify the virtual connection to which the cell belongs. These identifiers have only local significance, to avoid problem of unique global allocation. The VCI is local to each switch port; as each cell traverses a switch, the VCI is translated and assigned for the next link in the virtual connection.

The Generic Flow Control (GFC) field is to be used for unspecified flow control function. The Payload Type Identifier (PT) field indicates the type of information in the information field. The Cell Loss Priority (CLP) is used to provide guidance to the network in the event of congestion. A value of 0 indicates a cell of relatively higher priority which should not be discarded, unless no other alternative is available. A value of 1 indicates that the cell is subject to discard within the network. The Header Error-Control (HEC) field is an 8-bit error code that can be used to correct single-bit errors in the header and to detect double-bit errors.

My work centered around, designing circuits that will capture the 14 bits VCI's along with the CLP and PT, format them into ATM cell and store them in a temporary storage to be transmitted with a request/grant mechanism.

Collecting VCI's:

The first task was to come up with a design that will capture the VCI's. On the transmitter side, the VCI, CLP, and PT come at the same time, so they are collected at the same time into a 16-bit register. Two 16 bits entries are concatenated into 32 bits and then formatted into an ATM cell. The "measureinput" circuit unit (see schematic "measuresinput") consists of a 4-bit counter that keeps track of the states during
an ATM cell period, and a 5-bit counter that keeps track of the formation of new ATM cells. Combinational logic controls the timings for collecting and processing the VCI's.

On the receiver's side, the VCI's come at a different time than the CLP and the PT, so a different measure input controller has to be designed. The 4 bits of the PT and the CLP are clocked into a register. The bit 0 which is for the CLP is allowed to go through with the 14 bits of VCI and the 3 bits of PT are converted into 1 bit to make the 16 bits which are then forwarded. The process of formatting to ATM cell is same as the transmit VCIs. (see schematic measure input2).

The VCI sequence in the cell stream transmitted and/or received over the WAN is the basis for traffic measurements for the AN2/SONET Gateway. The hardware capturing the VCI from the cells in transit has been described. The VCIs are then placed into the payload area of temporary storage cells that are subsequently sent to a host on the AN2 network for permanent storage and later analysis.

The FIFO Control Unit:

The First In First Out (FIFO) control unit is a mechanism that controls the formatted VCIs (32 bit entries) in the FIFO without overwriting any valid entries. As soon as it receives any valid entry it requests that the entry be forwarded. When there is a grant from the next chip the entry is forwarded. A state machine controls the operation of the FIFO. The state machine monitors the validity of each of the registers within the FIFO. This prevent any erroneous entry due to a malfunctioning FIFO. If the FIFO is full, any new entries are discarded (see the "fifocontrol" and "TestFifo" schematic.).
Results:
The design generates two streams of valid ATM cell without the HEC byte. The payload contains 24 entries, each of which contains 14 VCI, bits, 1 CLP bit and 1 bit derived from 3 bits of PT. These circuits will operate at 25mhz when implemented in Xilinx Field Programmable Gate Arrays (FPGAs). The simulation results show how the VCI, CLP, and the PT are collected and formatted into ATM cells. It also shows how they are stored in the temporary storage (FIFO Unit) and forwarded with the request/grant mechanism.

Future Work:
The design can easily be modified to simultaneously measure 3 different points in the data flow and generate 3 streams of ATM cells. (1 stream for each measurement point). Parts of these circuits are fairly general; for example, the FIFO control unit can be used for other circuits.
Fifo Control

clk    en1

reset_h    en2

cell_h

grant_h    en3

request_h

en5

oe1

oe2
measure input2

clk_cell2_h

count1

count2

en0_1

en0_2

en1

en2

en3_1

ten3_2

count

clock

count2