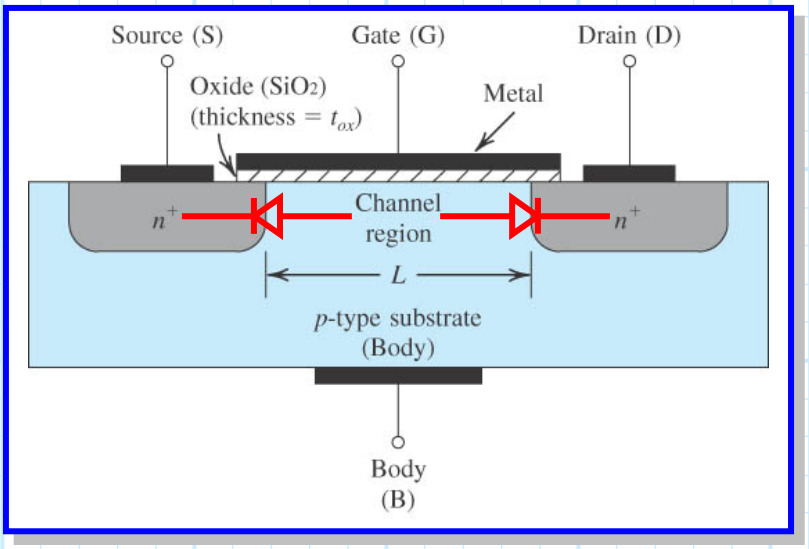
Creating a Channel for Current Flow

When we first look at an **NMOS** device, it appears that **no** current can flow from the Drain electrode to the Source electrode (or vice versa) as we must contend with two ***p-n* junctions**!



* Current seemingly cannot flow **into** channel from the Drain, as this would require current flowing from an *n*-type (cathode) region into a *p*-type (anode) region.

* Likewise, current cannot flow **into** channel from the Source, as this would require current flowing from an *n*-type (cathode) region into a *p*-type (anode) region.

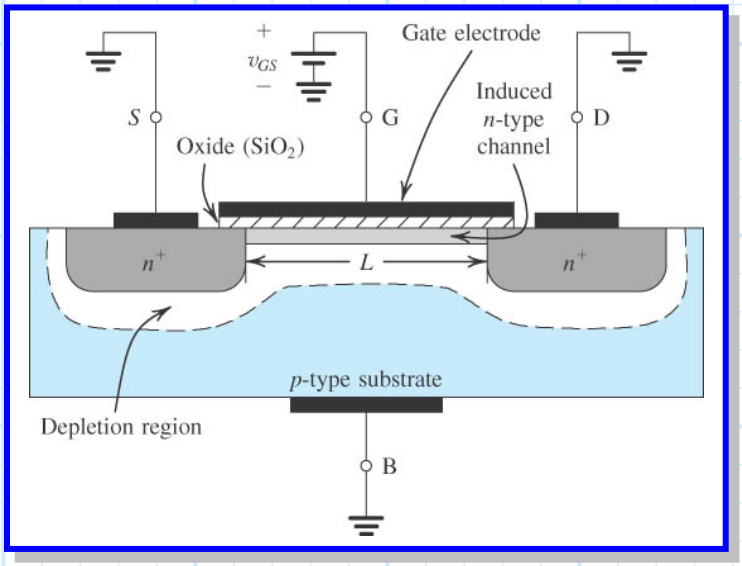
* Recall that we have previously determined that current **cannot** flow into (or out of) the channel from (into) the **gate**, as the SiO2 layer is a very good **insulator**!

Q: *Pardon me, but this NMOS device does **not** appear to be particularly **useful**. I mean, what good is a device if **no** current can flow into it?*

A: An NMOS device would indeed be useless **if** no current could flow from drain to source. However, we can **modify** the channel so that this current **can** indeed flow!

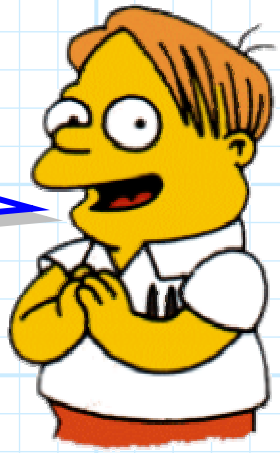
We must **induce a channel**—that is, create a thin layer of *n*-type Si connecting the source and drain!

To do this, we place a **positive voltage** at the **gate** electrode. This creates an **electric field** within the *p*-type substrate, which pushes the positively charged holes in the *p*-type substrate away from the gate electrode—a **depletion region** is formed in the Silicon under the gate!



The electric field under the gate electrode will **repel** positively charged holes, but will **attract** negatively charged free electrons!

Q: *I see! The minority carriers in the p-type substrate (i.e., **free electrons**) are attracted to the **gate** electrode!*



A: True! But we also find that many of the free electrons attracted to the gate come from the **heavily doped** n^+ wells under the source and drain electrodes.

* Of course, there is a Silicon Dioxide **insulator** separating the gate electrode and the Silicon substrate, so the free-electrons attracted by the gate electrode simply "**pile up**" at the **top** of the Silicon substrate, just **under** the SiO_2 layer.

* The result is an "**inversion layer**"—*A* **thin** layer in the *p*-type silicon where the majority carriers are actually **free electrons**!

* This inversion layer forms a ***n*-type conducting channel** connecting the *n+* Silicon well under the **drain** to the *n+* Silicon well under the **source**. By applying a positive voltage to the gate, we have **induced a conducting channel**!

In other words, current flowing from drain to source **no longer** encounters any ***p-n* junctions**!

Q: *So, will **any** positive gate voltage suffice for inducing a channel, **or** must this gate voltage be somehow sufficiently **large**?*

A: The later. The gate voltage must be **sufficiently large** to create an inversion layer—it must be sufficiently large to **induce** a conducting channel.

In fact, the voltage value must exceed some **threshold**.

First some **definitions**:

v_G = The gate electrode potential with respect to ground.

v_S = The source electrode potential with respect to ground.

$v_{GS} = v_G - v_S$ = The gate electrode potential with respect to the source.

We find that for a channel to be induced with in an **NMOS** device, the voltage v_{GS} must exceed a **threshold voltage**:

$$v_{GS} > V_t \quad \text{to induce an NMOS channel}$$

Moreover, we find that the amount by which v_{GS} **exceeds** the threshold voltage is a **very important** parameter for determining NMOS behavior. We call this value the **excess gate voltage**—this value is **very important**!

$$v_{GS} - V_t \doteq \text{excess gate voltage}$$

Thus, we can say:

$$v_{GS} - V_t > 0 \quad \text{to induce an NMOS channel}$$