Example: CMOS Logic Gate Synthesis

Problem: **Design** a CMOS digital circuit that realizes the Boolean function:

$$Y = \overline{A + B} + \overline{A}\,\overline{C}$$

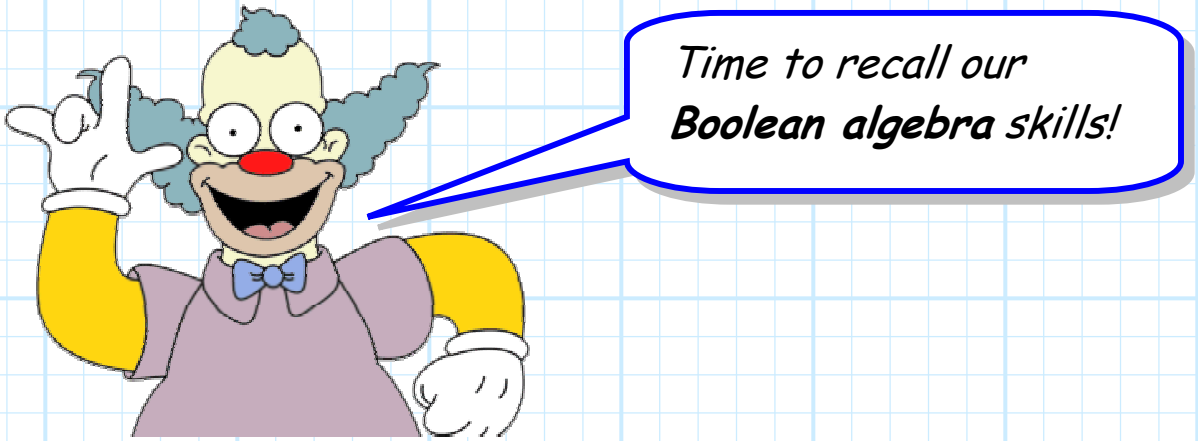
Solution: Follow the steps of the **design synthesis** handout!

Step1: Design the PDN

First, we must **rewrite** the Boolean function as:

$$\overline{Y} = f(A, B, C)$$

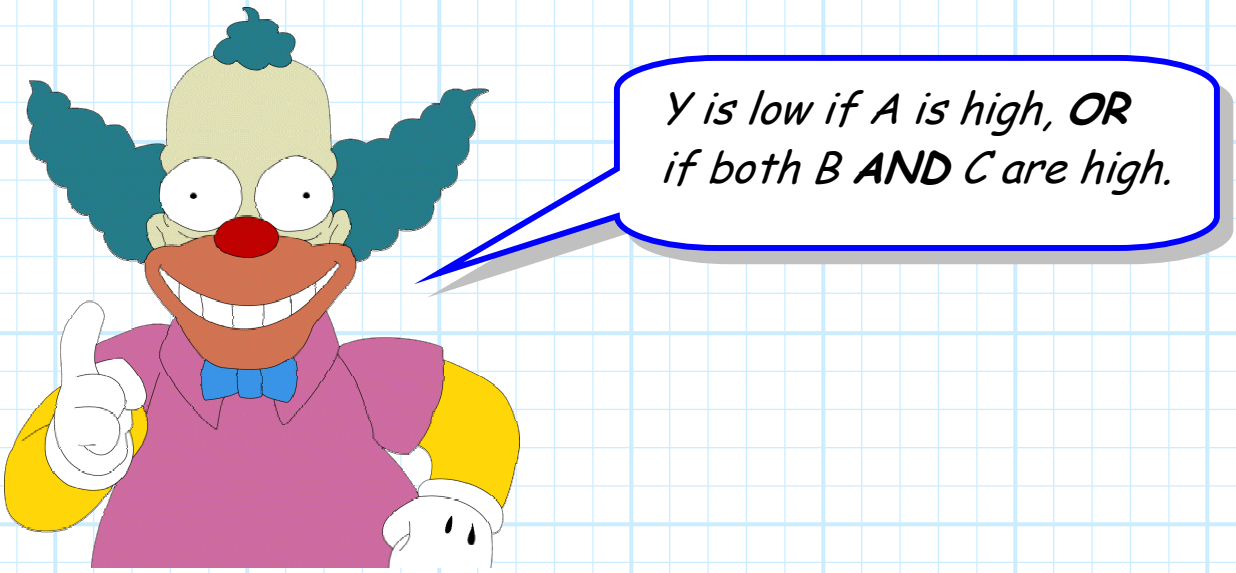
In other words, write the **complemented output** in terms of **un-complemented inputs**.



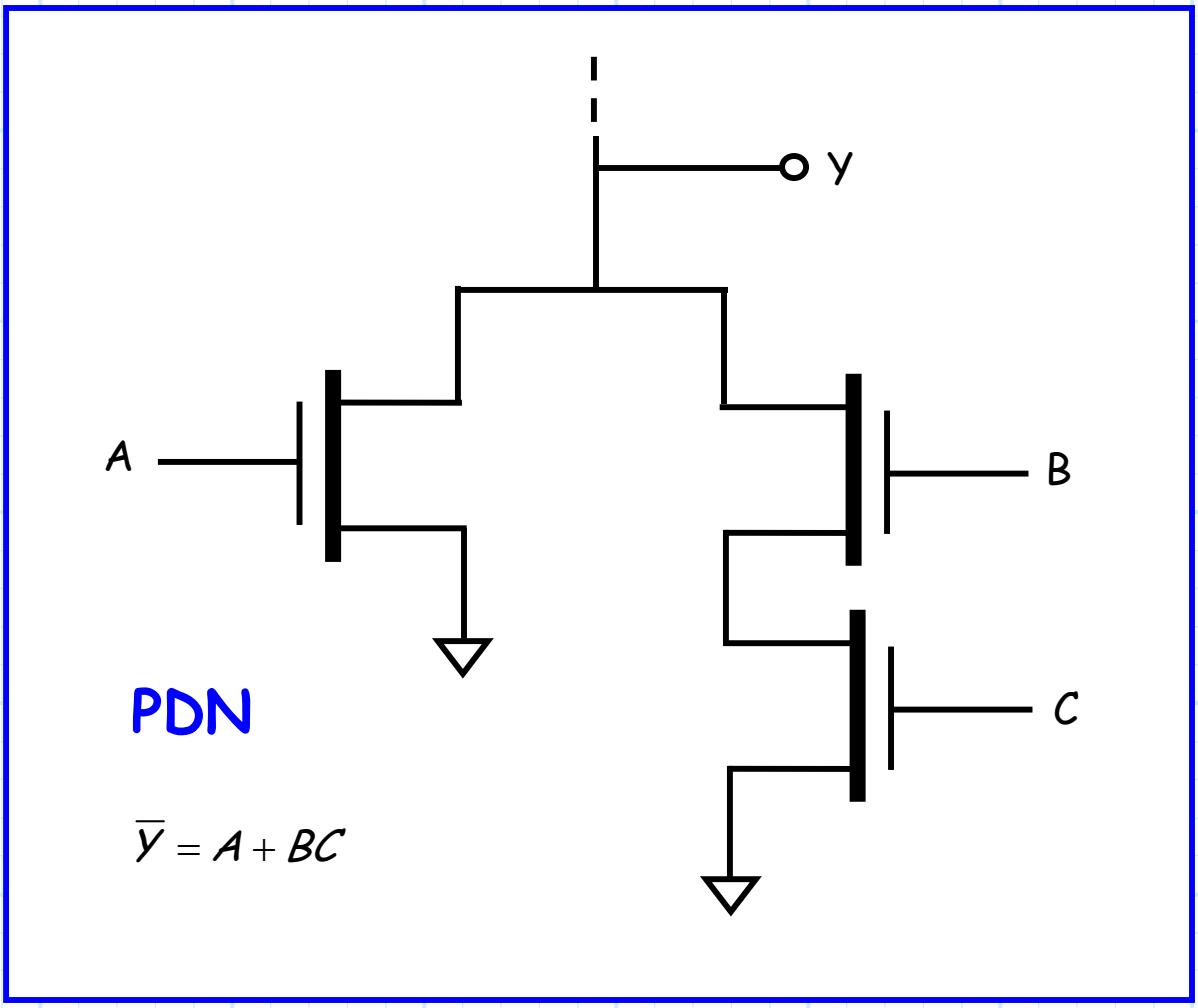
We must first complement this equation, and then apply **DeMorgan's Theorem** (several times!).

$$
\begin{aligned}
Y &= \overline{A+B} + \overline{A}\,\overline{C} \\
\overline{Y} &= \overline{\overline{A+B} + \overline{A}\,\overline{C}} \\
&= \left(\overline{\overline{A+B}}\right)\left(\overline{\overline{A}\,\overline{C}}\right) \\
&= (A+B)\left(\overline{\overline{A}} + \overline{\overline{C}}\right) \\
&= (A+B)(A+C) \\
&= AA + AC + BA + BC \\
&= A(A+B+C) + BC \\
&= A + BC
\end{aligned}
$$

Logically, this result says:



We can thus realize this logic with the following **NMOS** PDN:



Step2: Design the PUN

First, we must **rewrite** the Boolean function as:

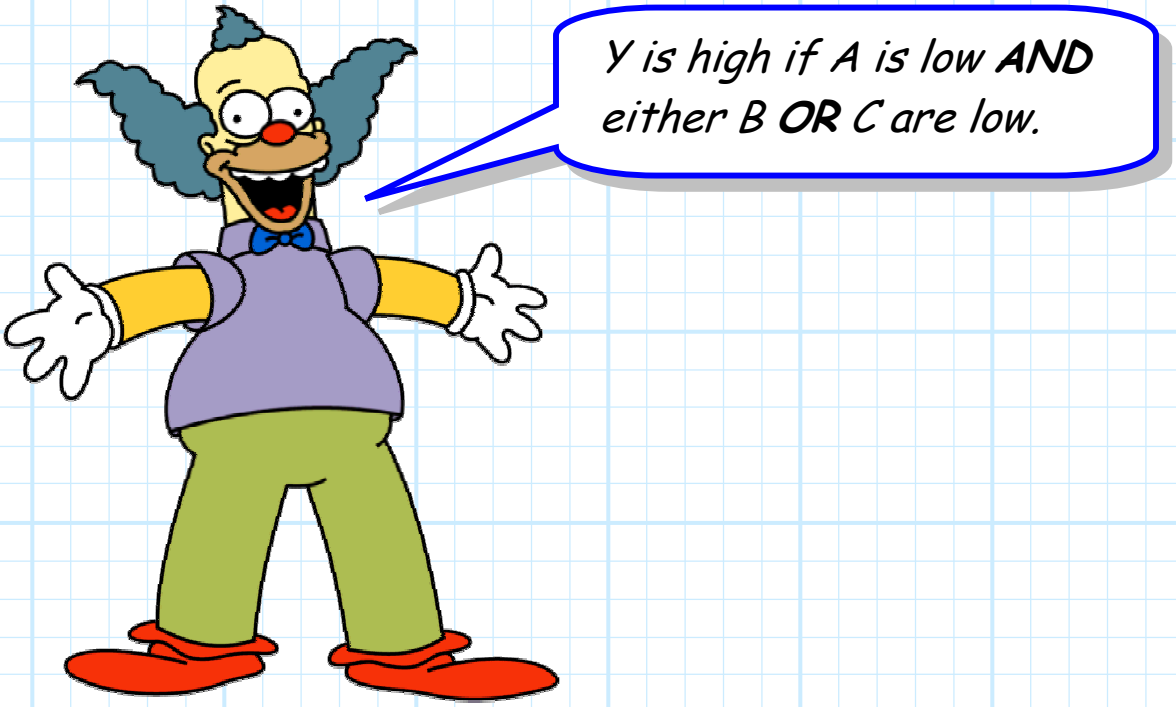
$$Y = f\left(\overline{A}, \overline{B}, \overline{C}\right)$$

In other words, write the **un-complemented output** in terms of **complemented inputs**.

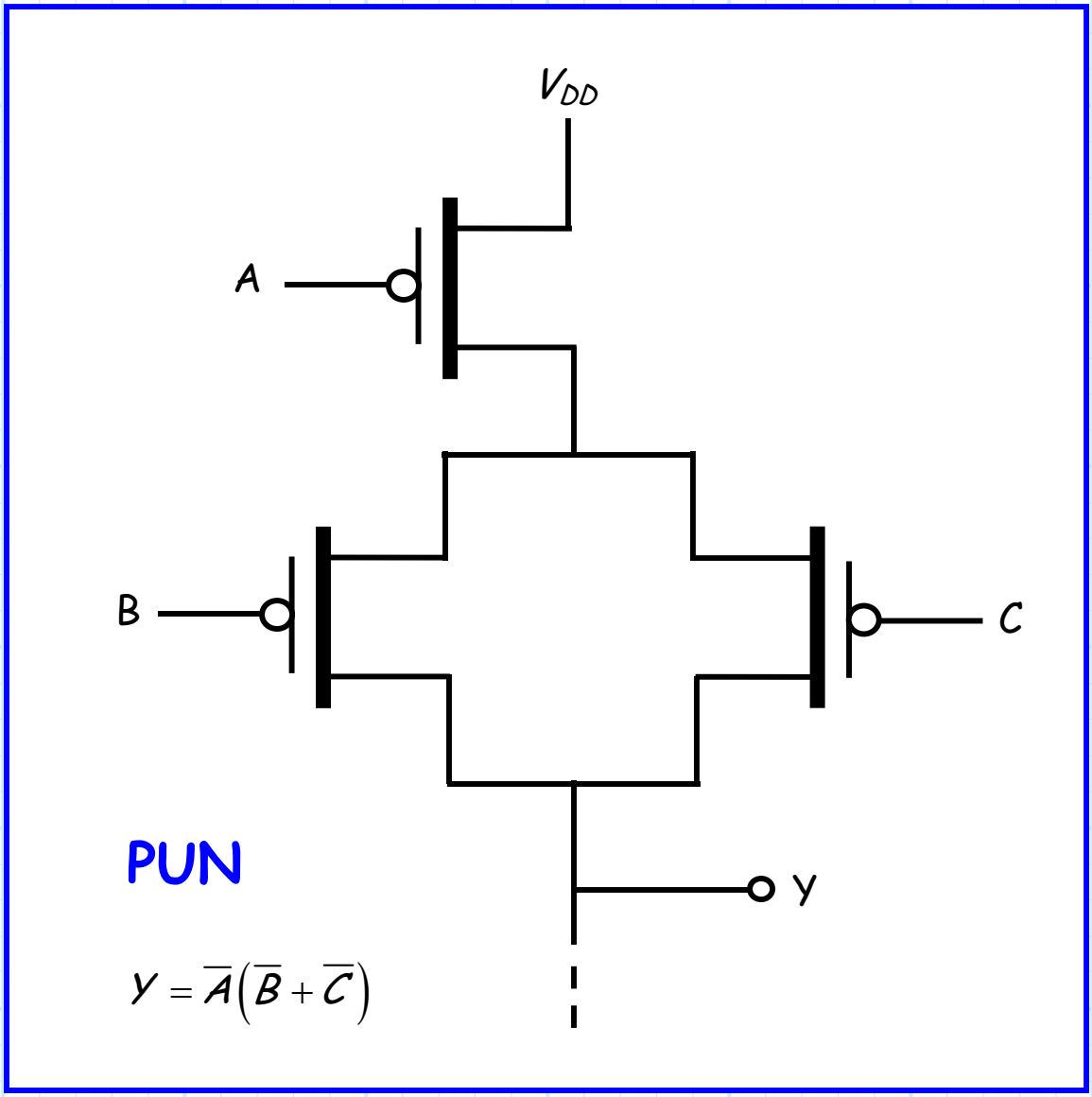
Again, using **DeMorgan's Theorem**:

$$\begin{aligned} Y &= \overline{A + B} + \overline{A}\,\overline{C} \\ &= \overline{A}\,\overline{B} + \overline{A}\,\overline{C} \\ &= \overline{A}\left(\overline{B} + \overline{C}\right) \end{aligned}$$

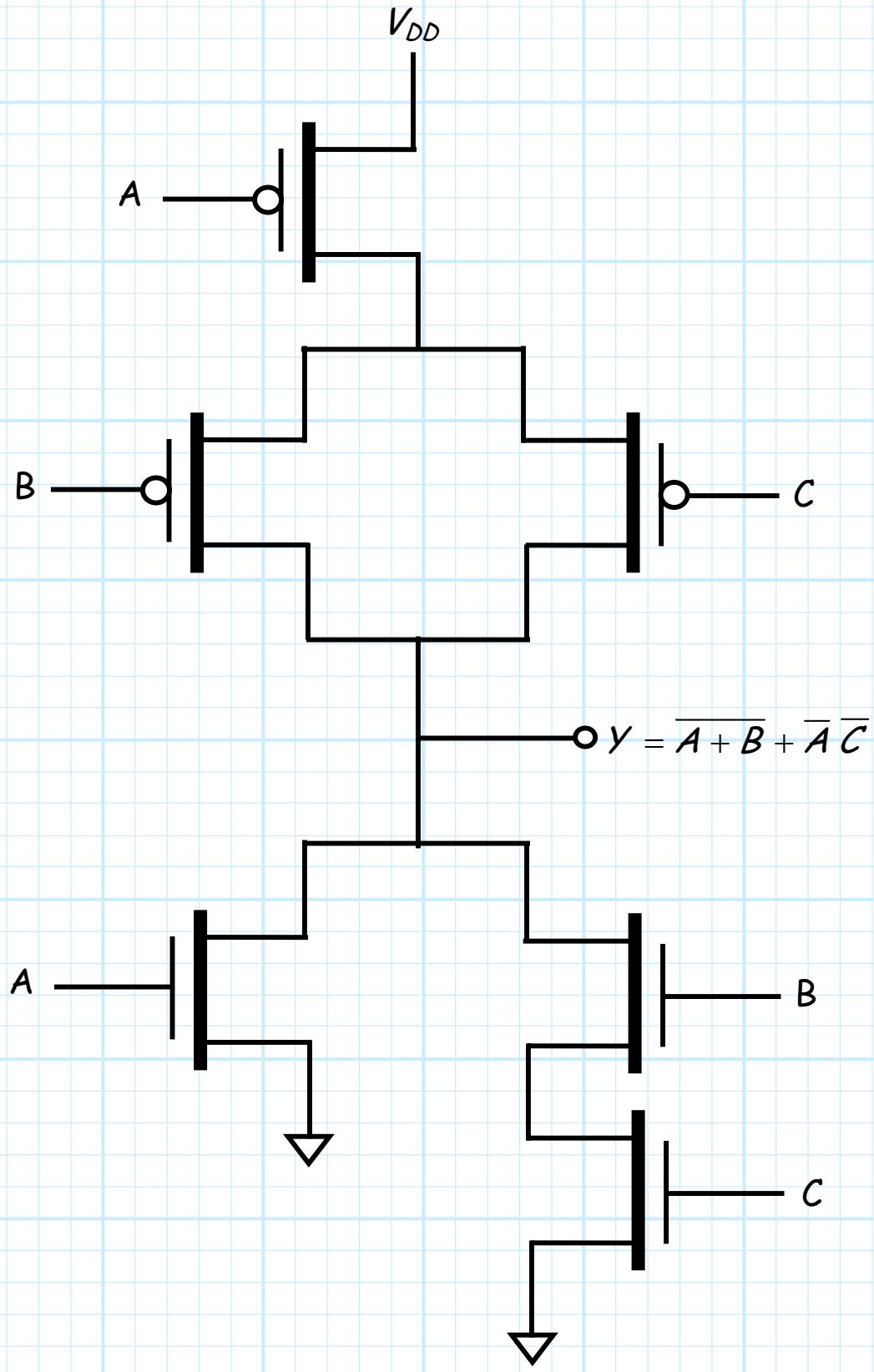
Logically, this result says:



We can thus realize this logic with the following **PMOS** PUN:



Thus, the **entire** CMOS realization is:


V_{DD}
A
B
C
$Y = \overline{A + B + \overline{A}\,\overline{C}}$
A
B
C